INTL3524&3528 Product Brief

1. Description

INTL352X is a family of I2C/I3C Multiple Port Hub devices featuring two I2C/I3C Master Side Ports and up to eight I2C/I3C Slave Side Ports. An INTL352X device provides connectivity to up to two masters, and up to eight slaves. By cascading and duplicating the INTL352X, the user builds an INTL352X Hub Network to provide connectivity to a number of devices, with extended reach distance, and running with different level of I2C, I3C, and SMBus protocols.

In an INTL352X device, each of Master Side Port is associated with an on-chip I2C/I3C slave interface. Each I2C/I3C interface accesses on-chip registers. Master and Master communication is achieved with shared registers and intra-port IBI channels.

One of the two Master Side Ports is selected to connect to a 1: N Hub network, which allows the selected master to get access to the enabled Slave Side Ports in the Hub network. The master selection multiplexer allows the two masters to share the downstream I2C/I3C network.

The 1: N I2C/I3C Hub network allows the management of the I2C/I3C hierarchy with expansion to up to eight Slave Side Ports. The expanded ports allow the system to reduce the load that the selected master sees at any moment. The Hub network maintains software level transparently. All devices connected to the Hub Slave Side Ports are accessed the same way as if all ports directly connected as if the Hub network does not exist. The Hub network also allows physical segmentation of the I2C/I3C hierarchy employing on the fly connecting and disconnecting to any of the expanded ports.

Each Slave Side Port is associated with a Bus Agent. This Agent independently receives or transmits legacy SMBus transactions and allows SCL Stretching within the SMBus segment behind the Slave Side Port. When the SMBus Agent is active, the Agent is engaged directly with the Slave Side Port and the Hub Network to the port is disconnected.

2. Features

- Two Master Side Ports
- Up to eight Slave Side Ports
- On-Chip I2C/I3C Slave Interface
- Master Side Port multiplexer

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- Master switching via in-band I2C/I3C commands or pin selection
- Master and Master communication and messaging support
- Hot Join support
- Support both I2C and I3C Basic 1.0 Protocol
- All ports support 1.0 to 1.8V I2C/I3C compatible operation
- All ports support I2C Open-Drain only operation up to 3.3V
- JEDEC SPD/Module Management Bus Context support
- Master to Slave analog switch mode support
- Analog switch and re-driving support
- Mixed I2C/I3C Bus support
- IBI and IBI Optimization support
- Single 3.3V power supply
- Master-Slave Level shifting support
- On-Chip Voltage Regulators or direct platform connection of IO supplies
- SMBus transaction agent for SMBus compatibility
- SMBus SCL stretching support
- SMBus SCL stretching support in Open-Drain Only Operation
- Network partition support
- Mixed transparent and non-transparent bridging

3. Application

- DIMM I3C fan-out
- I3C/I2C/SMBus compatibility
- I3C Port Expansion and Level adaptation
- I3C Topology Management
- I3C Signal Integrity Management

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4. Functional Diagram

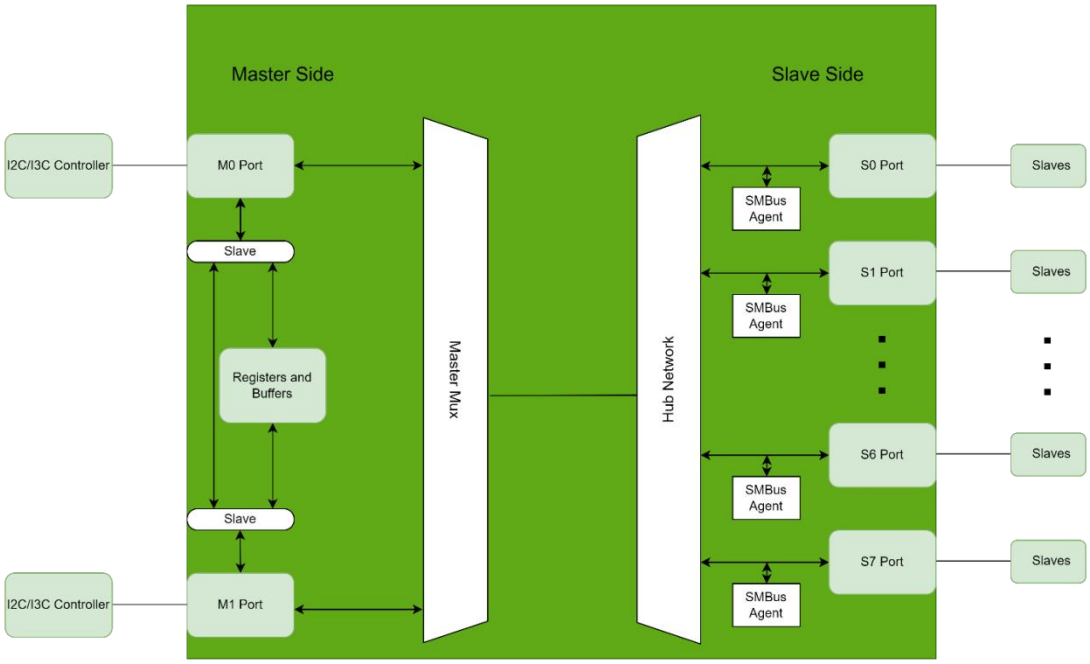

Figure 1 Function Diagram